WHAT IS CLAIMED IS:

1. A computer chipset comprising:

an identifier module configured to add a first sequence identifier to each transaction in a first ordered sequence of transactions and to add a second sequence identifier to each transaction in a second ordered sequence of transactions, and to combine the first and second ordered sequences of transactions into a combined ordered sequence of transactions; and

a router that separates the combined ordered sequence of transactions into two ordered queues based on the sequence identifiers associated with the transactions.

2. The computer chipset of claim 1, further comprising an output port configured to send the transactions in the two ordered queues to a data bus in an order that reduces the time required to complete the transactions.

3. The computer chipset of claim 1 in which the first sequence of transactions comprise transactions from a first input/output device, and the second sequence of transactions comprise transactions from a second input/output device.

4. The computer chipset of claim 3 in which the transactions comprise write transactions.

5. The computer chipset of claim 4 in which the combined ordered sequence of transactions follow PCI ordering rules.

6. The computer chipset of claim 3 in which the transactions comprises read transactions.

7. A method comprising:

receiving first and second ordered sequences of transactions from first and second devices, respectively;

adding a first sequence identifier to each transaction in the first sequence;

combining the first and second ordered sequences of transactions with respective identifiers into a third ordered sequence of transactions; and

sending the third ordered sequence of transactions over an interface that follows ordering rules.

8. The method of claim 7, further comprising adding a second sequence identifier to each transaction in the second sequence.

9. The method of claim 8, further comprising routing the transactions in the third ordered sequence to two ordered queues based on the sequence identifiers associated with the transactions.

10. The method of claim 9, further comprising executing the transactions in the ordered queues in an order that reduces the time required to complete the transactions.

11. Apparatus comprising

a port configured to receive first and second ordered sequences of transactions from first and second devices, respectively;

an identifier adding component configured to add a first sequence identifier to each transaction in the first sequence and to add a second sequence identifier to each transaction in the second sequence, and to combine the first and second ordered sequences of transactions with their respective identifiers into a third ordered sequence of transactions; and

a router configured to separate the transactions in the third ordered sequence into two ordered queues of transactions based on the sequence identifiers associated with the transactions.

12. The apparatus of claim 11, further comprising an execution component configured to execute the transactions in the two ordered queues in an order that reduces the time required to complete the transactions.

13. The apparatus of claim 12, further comprising an interface that follows an ordering rule, the third ordered sequence of transactions being transmitted from the identifier adding component to the router through the interface.

14. The apparatus of claim 11 in which the transactions comprise write transactions.

15. The apparatus of claim 14, further comprising a memory, the write transactions writing units of data to the memory in a predetermined order.

16. The apparatus of claim 15, further comprising another memory, the first sequence of transactions writing units of data to the memory in a predetermined order, the second sequence of transactions writing units of data to other memory in a predetermined order.

17. The apparatus of claim 11 in which the transactions comprise read transactions.

18. The apparatus of claim 11 in which the first and second ordered sequence of transactions follow PCI ordering rules.

19. The apparatus of claim 18 in which the third ordered sequence of transactions follow PCI ordering rules.

20. Apparatus comprising:

input/output devices, each of which sends an ordered stream of transactions;

a circuit configured to combine the ordered streams of transactions sent from the input/output devices into a combined ordered stream of transactions, the circuit adding sequence identifiers to each transaction to identify the origin of the transaction; and

a router that routes the transactions in the combined ordered stream to ordered queues based on the sequence identifiers associated with the transactions.

21. The apparatus of claim 20 in which the transactions comprise write transactions that write units of data to memory devices in predetermined orders.

22. The apparatus of claim 21, further comprising a processor that processes the write transactions in the ordered queues in an order that reduces the time required to complete the write transactions.

23. A computer input/output hub comprising:

an input port configured to receive a combined ordered sequence of transactions that includes transactions from first and second ordered sequences of transactions, each transaction

in the first ordered sequence having an associated first sequence identifier, each transaction in the second ordered sequence having an associated second sequence identifier; and

a router that separates the combined ordered sequence of transactions into two ordered queues based on the sequence identifiers associated with the transactions.

24. The computer input/output hub of claim 23 wherein the first ordered sequence of transactions obey PCI ordering rules.

25. The computer input/output hub of claim 24 wherein the second ordered sequence of transactions obey PCI ordering rules.

26. The computer input/output hub of claim 25 wherein the transactions in the two ordered queues are sent to a data bus that has an ordering rule more relaxed than PCI ordering rules.

27. The computer input/output hub of claim 26 wherein the transactions in the two ordered queues are sent to the data bus in an order that reduces the amount of time required to complete the transactions.